In the Claims:

1. (currently amended) A semiconductor device, comprising:

a layer of dielectric material overlying a substrate;

a dielectric pedestal disposed within and integral to said layer of dielectric material located above remaining portions of said layer of dielectric material ~~and integral to a substrate~~ and having first sidewalls;

a semiconductor channel region located above said dielectric pedestal and having second sidewalls; and

source and drain semiconductor regions disposed adjacent said first sidewalls of said dielectric pedestal and partially overlying said remaining portions of the layer of dielectric material opposing said channel region and each substantially spanning one of said second sidewalls.

2. (original) The semiconductor device as recited in Claim 1 wherein said first and second sidewalls are substantially coincident.

3. (original) The semiconductor device as recited in Claim 1 wherein each of said source and drain regions further substantially spans one of said first sidewalls.

4. (original) The semiconductor device as recited in Claim 1 wherein said dielectric pedestal and said substrate comprise at least a portion of a silicon-on-insulator (SOI) substrate.

5. (original) The semiconductor device as recited in Claim 1 wherein said channel region, said dielectric pedestal and said substrate comprise at least a portion of a silicon-on-insulator (SOI) substrate.

6. (original) The semiconductor device as recited in Claim 1 wherein said dielectric pedestal is at least a portion of a buried oxide (BOX) layer located in said substrate.

7. (original) The semiconductor device as recited in Claim 1 further comprising a silicide layer over at least portions of said source and drain regions.

8. (original) The semiconductor device as recited in Claim 1 further comprising a gate structure including a gate oxide located above said channel region and a gate electrode located above said gate oxide.

9. (original) The semiconductor device as recited in Claim 8 wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm.

10. (original) The semiconductor device as recited in Claim 1 wherein said channel region has a length ranging between about 2 nm and about 100 nm.

11. (original) The semiconductor device as recited in Claim 1 wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.

Claims 12-25 (Canceled)

26. (currently amended) An integrated circuit device, comprising:

a semiconductor device, including:

a layer of dielectric material formed over a substrate;

a dielectric pedestal within and integral to said layer of dielectric material and located above remaining portions of said layer of dielectric material ~~and integral to a substrate~~

and having first sidewalls;

a channel region located above said dielectric pedestal and having second sidewalls; and

source and drain semiconductor regions disposed adjacent the first sidewalls of said dielectric pedestal and disposed partially overlying said remaining portions of said dielectric layer and opposing said channel region and each substantially spanning one of said second sidewalls;

an interlevel dielectric layer located over said semiconductor device; and

vias spanning said interlevel dielectric layer and contacting said source and drain regions.

27. (original) The integrated circuit device as recited in Claim 26 wherein said first and second sidewalls are substantially coincident.

28. (original) The integrated circuit device as recited in Claim 26 wherein each of said source and drain regions further substantially spans one of said first sidewalls.

29. (original) The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate.

30. (original) The integrated circuit device as recited in Claim 26 wherein said channel region, said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate.

31. (original) The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal is at least a portion of a buried oxide (BOX) layer located in said substrate.

32. (original) The integrated circuit device as recited in Claim 26 wherein said semiconductor device includes a silicide layer over at least portions of said source and drain regions.

33. (original) The integrated circuit device as recited in Claim 26 wherein said semiconductor device includes a gate structure having a gate oxide located above said channel region and a gate electrode located above said gate oxide.

34. (original) The integrated circuit device as recited in Claim 33 wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm.

35. (original) The integrated circuit device as recited in Claim 26 wherein said channel region has a length ranging between about 2 nm and about 100 nm.

36. (original) The integrated circuit device as recited in Claim 26 wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.